CHANGES TO THE SPECIFICATION

Please substitute the following marked up paragraph(s) for the paragraph(s) now appearing in the currently filed specification:

Paragraph at page 9, lines 9-15:

The portion indicated by 23c and having a width W1, shown in Fig. 3, which is provided in the conductor plate 23 between the opposing slots 24 and 25, becomes a propagation area in which a high-frequency signal having a desired propagation frequency fb is made to propagate. Further, the portions indicated by 23a and 23b on both sides, which sandwich the propagation area 23c, become cut-off areas.

Paragraph at page 19, line 1 to page 20, line 7:

Fig. 7 is a perspective view in a state in which the circuit substrate 30 is placed on the lower conductor plate 44. Fig. 8 is a plan view of the circuit substrate 30 shown in Fig. 7. This VCO is such that a resonator and a variable capacitive element are provided in the high-frequency amplifier shown in Fig. 1B. In ~~Fig. 7~~ Figs. 7 and 8, reference numeral 61 denotes a thin-film resistor, with the termination portion of the slot 14 formed on the top surface of the circuit substrate 30 being formed into a tapered shape and this thin-film resistor 61 being provided thereon. Reference numeral 74 denotes another slot provided on the top surface of the circuit substrate 30 and, as will be described later, a slot is also provided on the back-surface side of the circuit substrate 30 with the circuit substrate 30 interposed in between, forming the planar dielectric line. Reference numeral 60 denotes a variable capacitive element mounted in such a manner as to be extended over a slot 74, whose capacitance varies according to an applied voltage. As this variable ~~capacitive~~ capacitance element, a variable ~~capacitive~~ capacitance capacitor disclosed in Japanese Unexamined Patent Publication No. 5-74655, and a conventional variable ~~capacitive~~

capacitance diode may be used. Reference numeral 64 in the figure denotes a section where no conductor is formed, for providing a dielectric resonator, provided on the top surface of the circuit substrate 30 and, together with the opposing conductor non-formation section for a dielectric resonator on the back-surface side of the circuit substrate 30 with this substrate interposed in between, dorms a dielectric resonator of the TE010 mode in this portion. The remaining construction is the same as that of the first embodiment, and the top of the circuit substrate 30 shown in ~~Fig. 7~~ Figs. 7 and 8 is covered by an upper-part conductor plate.

Paragraph at page 20, line 8 to page 21, line 21:

~~Fig. 8 is a plan view of the circuit substrate 30 shown in Fig. 7.~~ Fig. 9 is a view showing the construction of the back-surface side of the circuit substrate 30. However, Fig. 9 is a view when the circuit substrate 30 is not viewed from the back-surface side, but viewed from the top surface thereof. As described above for Figs. 7 and 8, by forming the slots 14, 24, 74, 15, 25, and 75 on both main surfaces of the circuit substrate 30 with a dielectric plate interposed therebetween, three planar dielectric lines are constructed, and further, no conductor is formed at sections 64 and 65 so as to provide a dielectric resonator, thus a dielectric resonator of the TE010 mode having a large effect of trapping an electromagnetic field is constructed in this portion. Grooves of the upper and lower conductor plates are made to oppose each other to form a space section in three mounting sections in each of the planar dielectric line, the slot line, and the FET 30, and the periphery of the section where the coplanar lines 31 and 32 are formed. In this way, a band-reflection-type oscillator is constructed. Here, in the case where the specific dielectric constant of the dielectric plate is 24 and the thickness is 0.3 mm, if the diameter of the conductor non-formation sections 64 and 65 for a dielectric resonator is set at 1.7 mm, the resonance frequency thereof can be set to 60 GHz. Since this resonator and the planar dielectric line are not electromagnetically coupled to each other by merely bringing them close to each other, a very small cut-out section for coupling, indicated by C in Fig. 8, is

formed. A cut-out section, which is as small as the width being about 0.2 to 0.3 mm and the depth being about 0.05 to 0.1 mm, makes it possible to obtain sufficient coupling. With this construction, if the capacitance of the variable capacitive element 60 is varied, the impedance of the planar dielectric line, including the slot 74, varies, causing the resonance frequency of this planar dielectric line to vary. As a result, the resonance frequency of the dielectric resonator coupled to this line varies, making it possible to vary the oscillation frequency of the VCO.

Paragraph at page 23, lines 2-9:

According to the invention ~~of claim 1~~, since the space between the planar dielectric line and the electronic components is connected via the line-conversion conductor pattern and the slot line, it is possible to perform integration by reducing the signal loss in the coupled section of the planar dielectric line and the electronic components and while maintaining a low loss characteristic, which is a feature of the planar dielectric line.

Paragraph at page 23, lines 10-21:

According to the invention ~~of claim 2~~, when the signal is propagated from one planar dielectric line of the two planar dielectric lines to the other planar dielectric line, the signal is converted into the mode of the slot line at the midpoint by the line-conversion conductor pattern and the slot line, and signal conversion is performed by the electronic components, and then the signal is returned to the mode of the planar dielectric line via the line-conversion conductor pattern. Therefore, signal conversion using electronic components is made possible with a construction with a small energy conversion loss while performing the propagation of a signal using the planar dielectric line.

Paragraph at page 23, line 22 to page 24, line 4:

According to the invention ~~of claim 3~~, impedance matching is obtained between the line-conversion conductor pattern and the electronic components, and the loss in the connection section of the slot line and the electronic components is reduced.

Paragraph at page 24, lines 5-9:

According to the invention ~~of claim 4~~, impedance matching is obtained between the line-conversion conductor pattern and the planar dielectric line, and the slot line, thereby suppressing unwanted reflection and reducing the transmission loss caused by line conversion.